REMARKS

The Examiner is thanked for the performance of a thorough search.

OATH/DECLARATION

The Oath/Declaration has been objected to as allegedly failing to provide a full mailing address for inventor Garakani. Attached is a copy of the Response to the Notice to File Missing Parts that was filed on October 27, 2000 and which was received by the U.S. PTO on October 31, 2000, as indicated by the stamp from OIPE on the copy of the postcard included with the copy of the Response. The Response includes a copy of the complete and fully executed Declaration, and as indicated by the portions highlighted in the attached copy in the signature block for inventor Mehryar Garakani, a full and complete mailing address is listed after "post office address" along with the residence, which is different from the mailing address.

37 CFR 1.63(c) states:

> "Unless such information is supplied on an application data sheet in accordance with § 1.76, the oath or declaration must also identify:
>
> (1) The **mailing address**, and the **residence** if an inventor lives at a location which is different from where the inventor customarily receives mail, of each inventor; (emphasis added.)

The signature block for inventor Mehryar Garakani provides his **mailing address** as "P.O. Box 6189, Santa Barbara, California 93160" and provides his **residence** as "Los Angeles, California." The signature blocks for inventors Clare Chu and Kenneth E. Mueller, II, also include full and complete mailing addresses.

Thus, the Applicant respectfully submits that the Declaration as filed on October 27, 2000 with the Response to the Notice to File Missing Parts fully complies with 37 CFR 1.63(c), and therefore, the objection to the Declaration in the Office Action is rendered moot in light of the full and complete mailing address provided in the Declaration for inventor Garakani.

SPECIFICATION

The specification has been objected to because of an informality, namely the lack of a serial number for the co-pending application filed on May 31, 2000 that is referred to on

page 13. The paragraph on page 13, lines 4-14 has been amended to include the serial number of the co-pending application filed on May 31, 2000. No new matter is introduced. The Applicant respectfully submits that the amendment to add the serial number of the co-pending application addresses the objection to the specification raised in the Office Action.

The paragraph on page 13, lines 15-22, has been amended to include a reference to block 206 of FIG. 2A. The reference to block 206 is at the end of the sentence describing the content of block 206 in FIG. 2A. No new matter is introduced.

The paragraph on page 19, line 15 through page 20, line 7, has been amended to include a reference to block 262 of FIG. 2D. The reference to block 262 is at the end of the sentence describing the content of block 262 in FIG. 2D. In addition, a typographical error is corrected. No new matter is introduced.

DRAWINGS

The drawings have been objected to as allegedly failing to comply with 37 CFR 1.84(p)(5) because the drawings include the following reference signs that are not mentioned in the description: FIG. 2A, reference 206; FIG. 2D, reference 262; and FIG. 3, reference 350.

Regarding FIG. 2A, reference 206, the specification has been amended as described above to include a reference to block 206 at the end of the first sentence of the paragraph on page 13, lines 15-22, wherein the first sentence of that paragraph describes the content of block 206, as illustrated in FIG. 2A. No new matter is introduced. The Applicant respectfully submits that the amendment to the specification to add a reference to block 206 address the objection to FIG. 2A.

Regarding FIG. 2D, reference 262, the specification has been amended as described above to include a reference to block 262 at the end of the second sentence of the paragraph on page 19, line 15 through page 20, line 7, wherein the second sentence of that paragraph describes the content of block 262, as illustrated in FIG. 2D. No new matter is introduced. The Applicant respectfully submits that the amendment to the specification to add a reference to block 262 address the objection to FIG. 2D.

Regarding FIG. 3 and reference 350, the application as filed describes reference 350 as follows: "Connection 350 indicates the bypassing of route processor R2 314." (Application,

page 21, lines 1-2.) Thus, the Applicant respectfully submits that the objection to FIG. 3 and reference 350 is moot in light of the description of reference 350 in the application as filed.

STATUS OF CLAIMS

Claims 1-5, 7, 10-14, 16, 19, and 20 have been amended.

Claims 21-36 have been added.

No claims have been cancelled or withdrawn.

Claims 1-35 are pending in the application.

SUMMARY OF THE REJECTIONS REGARDING THE CLAIMS

Claims 1-4, 10-13, 19, and 20 have been rejected under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent Number 6,424,659 issued to Viswanadham et al. (" *Viswanadham* "). Claims 5-9 and 14-18 have been rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over *Viswanadham* in view of U.S. Patent Number 6,625,650 issued to Stelliga (" *Stelliga* "). The rejections are respectfully traversed.

A. CLAIM 1

(1) INTRODUCTION TO CLAIM 1

Claim 1 features:

"A method of determining a multilayer switching path for a flow between a source device and a destination device in a switched network, the method comprising the computer-implemented steps of:

determining a Layer 3 path and a Layer 2 path through the switched network from the source device to the destination device;

selecting each route processor of the switched network that is in the Layer 3 path and that appears on the Layer 2 path that is associated with the source device and the destination device and that leads to and emanates from the route processor;

selecting, for each selected route processor, a switch in the switched network that satisfies a pre-determined set of criteria as a relevant switch engine that multilayer switches the selected route processor;

creating and storing information that defines a multilayer switching path and that includes information identifying the source device, destination device, and each selected switch."

Thus, Claim 1 is an approach for determining the multilayer switching path between a source device and a destination device. The approach of Claim 1 address two needs as described in the Background section of the application, specifically the need for an approach "that can identify the path from a source device to a destination device in a switched network at multiple layers," and the "specific need for a way to carry out path tracing for multilayer switching paths for use in network management." (Application, page 5, lines 3-7.) This is in contrast to the use of switching, such as routing packets at Layer 3 through the use of routing algorithms, routing tables, next hops, etc. or Layer 3 path tracing and Layer 2 path tracing. (See Application, pages 3-4.) As noted in the Background section of the Application, the mere knowledge of the Layer 3 and Layer 2 paths may not provide certain path information, such as shortcuts in the Layer 3 and Layer 2 paths, whereby a packet may bypass certain Layer 3 and Layer 2 devices when multilayer switching is employed. (Application, page 4.) As a result, when multilayer switching is employed, there is a need for an approach to perform path tracing, such as that of Claim 1.

The approach of Claim 1 can be more fully understood by an example, such as the embodiment described with respect to FIG. 3 of the present application. The first step of Claim 1 is "determining a Layer 3 path and a Layer 2 path through the switched network from the source device to the destination device." Thus, in FIG. 3, the Layer 3 path between source device 302 and destination device 322 is Source 302-> R1 304->R2 314->Destination 322, which is represented by connections 330a, 330b, 330c. The Layer 2 path includes all the devices, routers, and switches shown in FIG. 3, as represented by connections 340a-340i.

The second step of Claim 1 is "selecting each route processor of the switched network that is in the Layer 3 path and that appears on the Layer 2 path that is associated with the source device and the destination device and that leads to and emanates from the route processor." Thus, in FIG. 3, the route processor that is selected is R2 314, because R2 314 is in the Layer 3 path represented by connections 330a, 330b, 330c and because R2 314 is in the Layer 2 path represented by connections 340a-340i.

The third step of Claim 1 is "selecting, for each selected route processor, a switch in the switched network that satisfies a pre-determined set of criteria as a relevant switch engine that multilayer switches the selected route processor." In FIG. 3, the relevant switch engine is SE1 312, which can be determined based on a pre-determined set of criteria, such as those described in Claim 2, namely that SE1 312 is a switch that is configured as a switch engine (e.g., as indicated by the "SE" designation), is associated with the selected route processor (e.g., R2 314), and is included in the Layer 2 path leading to and emanating from the selected route processor (e.g., connections 340c and 340f).

Finally, the last step of Claim 1 is creating and storing information that defines a multilayer switching path and that includes information identifying the source device, destination device, and each selected switch. Thus, in the switched network of FIG. 3, the information that is created and stored defines the multilayer switching path as connections 340a-340d, 350, and 340g-340i, and the information identifies source 302 (e.g., the source device), destination 322 (e.g., the destination device), and SE1 312 (e.g., the selected relevant switch engine).

(2) DISCUSSION OF *VISWANADHAM*

In contrast to Claim 1, in *Viswanadham* a "Multilayer switching device and associated technique enables simultaneous wire-speed routing as OSI layer 3 and wire-speed switching at layer 2, and support multiple interfaces at layer 1. Implementation may be embodied using one or more integrated circuits (ASIC), RISC processor, and software, thereby providing wire-speed performance on interfaces, in various operational modes." (Abstract.) Thus, the focus of *Viswanadham* is on providing "wire-speed" performance at layer 3 and layer 2, which means that the performance provided by *Viswanadham* is on par with performance occurring at the physical wire level, as opposed to the slower performance that typically occurs at the software level. Furthermore, the focus in *Viswanadham* is on the hardware implementation of the switch, such as in the described integrated circuits.

Viswanadham addresses the need for "a new generation of internetworking devices capable of gigabit speeds, but with the flexibility of previous software intensive products" that "typically exhibit poor system performance." (Col. 1, lines 29-31; lines 26-28.) This need is met by the "two-level distributed multilayer switch device 6" of FIG. 1, in which the

"Multilayer (e.g., both L2 and L3) switch fabric is entirely contained within single ASIC capable of switching 3M pps or more." (Col. 2, lines 30-34.) The balance of *Viswanadham* describes the architecture, circuit design, and operation of multilayer switch device 6. (*See* the BRIEF DESCRIPTION OF DRAWINGS, Col. 1, line 43 through Col. 2, line 14.) Note that the only network described in *Viswanadham* is that of FIG. 1, which is only briefly described and servers only to provide the context in which multilayer switch device 6 operates. (Col. 2, lines 18-29.) Therefore, the focus of *Viswanadham* is on the hardware design of a switch, in contrast to the use of the switch in a network and network operations, such as determining a multilayer switching path in a network.

(3) THE OFFICE ACTION'S CITATIONS FROM *VISWANADHAM*

The Office Action states that *Viswanadham* discloses "a method of determining a multilayer switching path (col. 2, lines 17-29)." However, the cited portion of *Viswanadham* merely describes Figure 1 to provide the context in which multilayer switch device 6 operates, namely that "multilayer switch device 6 couples local area network (LAN) workgroup hubs 2 through enterprise switching hub 4 to wide-are network (WAN) links through multiprotocol router 8." (Col. 2, lines 17-22.) *Viswanadham* then describes the advantages of the subject multilayer switch and possible implementations as: "Multilayer switch device 6 and associated technique enables simultaneous wire-speed routing at Layer 3 (L3), wire-speed switching at Layer 2 (L2), and support multiple interfaces at Layer 1 (L1), according to OSI reference model. System may be embodied using one or more integrated circuits (ASIC), RISC processor, and software, thereby providing wire-speed performance on various interfaces in various operational modes." (Col. 2, lines 22-29.)

Nowhere in the cited portion of *Viswanadham* is a "path" or anything equivalent to a path even mentioned, little less the disclosure of a "multilayer switching path" or a "method for determining" any kind of a path. Because the cited portion of *Viswanadham* merely describes the context for using multilayer switch device 6, its advantages and possible implementations, the Applicant is unable to determine what aspects of the cited portion of *Viswanadham* that the Office Action is relying upon to disclose a "method for determining a multilayer switching path" as recited in the preamble of Claim 1.

For this issue and many other issues, the Office Action does not specify exactly what in *Viswanadham* corresponds to or constitutes each element or feature of the claims. In an Office Action, "the particular part relied on must be designated as nearly as practicable ... The pertinence of each reference, if not apparent, must be clearly explained ..." 37 C.F.R. § 1.104; MPEP 707. The present citations to the references do not provide the Applicant with adequate notice or reasonable particularity with respect to the basis of the rejections. Instead, large portions of the references are simply identified in a non-specific way. As a result, the Applicant has had to engage in guesswork to determine the basis of the rejection. No corresponding structure or functions are seen by the Applicant.

For example, the Office Action states that *Viswanadham* discloses "determining a Layer 3 path and a Layer 2 path through the network (col. 2, lines 31-67, wire-speed routing at layers 2 and 3) from the source device to the destination device (figure 9B)." However, as *Viswanadham* is best understood by the Applicant, the rationale of the Office Action is technically incorrect. The cited portion of *Viswanadham* describes that the "system architecture comprises two-level distributed multilayer switch," thereafter providing details of the hardware architecture of the multilayer switch device 6. (Col. 2, lines 31-42). Then *Viswanadham* discusses Figures 2A and 2B, which are described as "block diagrams of first- and second-level switch respectively." (Col. 1, lines 45-46.)

Specifically, Figure 2A describes a first-level switch 22, while Figure 2B describes a second-level switch or cross-bar interconnection 18 that couples multiple first-level switches 22. (Col. 2, lines 43-55.) The remainder of the cited portion of *Viswanadham* describes that RISC processors 10, 12 that are provided in each switch element 22 execute software to provide standards-based dynamic routing, and non-real time activities, concluding by describing several preferred software functions. (Col. 2, lines 56-67.)

Thus, the cited portion of *Viswanadham* describes the internal architecture of a multilayer switch as comprising a second-level crossbar switch 18 that interconnects several first-level switches 22. Yet Claim 1 features "determining a Layer 3 path and a Layer 2 path through the switched network from the source device to the destination device." It is unclear to the Applicant how the description of the internal architecture of a multilayer switch can be considered to disclose the function of determining both a Layer 3 path and also a Layer 2 path between a source device and a destination device in a switched network.

Furthermore, contrary to the assertion of the Office Action, there is nothing in Figure 9B, which *Viswanadham* describes as illustrating "LAN arbiters interaction with datapath" (Col. 11, line 12), that can be identified by the Applicant as disclosing either a "source device" or a "destination device" as featured in Claim 1.

The Applicant notes that the parenthetical notation in the Office Action's citation of "wire-speed routing at layers 2 and 3" following "col. 2, lines 31-67 appears to be asserting that "wire-speed routing" is described in the cited portion, when in fact wire-speed routing fails to appear in the cited portion. However, wire-speed routing is mentioned in the previous paragraph (Col. 2, lines 17-29), and the Applicant will proceed based on the discussion of wire-speed routing in that paragraph.

As best understood by the Applicant, the Office Action appears to be asserting that the ability of multilayer switch device 6 to enable "wire-speed routing at Layer 3" and "wire-speed switching at Layer 2" (Col. 2, lines 23-24) is equivalent to determining a Layer 3 path and a Layer 2 path between the source device and destination device. However, the ability to route at Layer 3 and switch at Layer 2 is not the same as determining a path at Layer 3 and a path at Layer 2. At best, the functions of routing and switching determine the next step, or hop, from the current device at which a packet is located to the next device. This is quite different from determining the path between the source device and the destination device, which consists of many such steps or hops. As described in the Application (see pages 3-4), such path determination involves identifying the applicable Layer 3 and Layer 2 devices that are traversed by a packet at Layer 3 and Layer 2, respectively, which is called "Layer 3 path tracing" and "Layer 2 path tracing."

Furthermore, such path tracing is typically performed by a computer program, such as "traceroute" for Unix-based network computers or "tracert" for Windows-based network computers. (Application, page 12.) Such programs operate by sending packets with time limit values that are exceeded upon receipt at a gateway, so that the gateway returns a Time Exceeded message, thereby allowing the program to determine the device reached by the packet. In contrast, *Viswanadham* fails to describe anything in either the cited portion or elsewhere that functions to provide such path determination at any level, little less Level 3 and Level 2 between a source device and a destination device, as featured in Claim 1.

For at least these reasons, the Applicant respectfully submits that *Viswanadham* does not disclose, teach, suggest, or in any way render obvious "determining a Layer 3 path and a Layer 2 path through the switched network from the source device to the destination device" as featured in Claim 1.

Next, the Office Action states that *Viswanadham* discloses "selecting each route processor of the network that is in the Layer 3 path and that appears on a Layer 2 path that is associated with the source device and the destination device and that leads to and emanates from the route processor (col. 9, lines 58-67; col. 10, lines 1-67; figures 8A, 9A, L2 and L3 CAMs route cache)." Again, as noted above, the Office Action cites a over a column worth of material from *Viswanadham* along with two figures without providing reasonable particularity with respect to the basis of the rejections, and as a result, the Applicant has had to engage in guesswork to determine the basis for the rejection.

The cited portion of *Viswanadham* describes Figures 7B, 8A, 8B, and 9A, which illustrate the following portions of the multilayer switch device: Figure 7B - "RP processor 12 access to packet memory (PM) 16 through L2/L3 switch circuit 20" (Col. 9, lines 58-59); Figure 8A - "RP processor 12 access to L3CAM (route cache) memory 28" (Col. 10, lines 10-11); Figure 8B - "control memory 136 access through switch circuit 20" (Col. 10, lines 13-14); and Figure 9A - "RP processor 12 accesses L2CAM memory 142 through switch circuit 20" (Col. 10, lines 58-59). RP processor 12 is described as a "route processor (RP) 12," which preferably is a "NEC Vr4300 RISC microprocessor from MIPS family..." (Col. 8, lines 51-52.) The descriptions of Figures 7B, 8A, 8B and 9A detail the internal functioning of multilayer switch device 6 with respect to RP processor 12 that is included as part of first-level switch 22 (see Figure 2A).

Viswanadham uses the term "route processor" to refer to a particular microprocessor that is included in the first-level switch 22. In addition to RP processor 12, first-level switch 22 also includes a RISC network management processor 10. (Figure 2A.) *Viswanadham* also refers to RP processor 12 as "switch processor 12." (Figure 4.) Thus, *Viswanadham* is consistent in describing "route processor 12" as being one of at least two processors that are contained within a switch, such as first-level switch 12.

However, the term "route processor" in Claim 1 refers to a device that performs routing, such as routers, and the Application includes several specific examples of route

processors as routers, such as Router R 106 in FIG. 1 and router 508 in FIG. 5A, FIG. 5B, and FIG. 5C. Therefore, the "route processor" referred to in *Viswanadham* is not the same as the "route processor" as used in Claim 1.

In addition, L3CAM is described with reference to "L3CAM (route cache) memory 28" of Figure 8A (Col. 10, lines 10-11), and L2CAM is described with reference to "L2CAM memory 142" of Figure 9A (Col. 10, lines 58-60), in which "CAM" stands for "Content Addressable Memory" (Col. 10, line 59.). Thus, the "L2 CAM" and "L3 CAM" are clearly described as types of memory that are included as part of the multilayer switch device 6. As best understood by the Applicant, it appears that the Office Action is equating the "L3CAM (route cache)" to the Layer 3 path and the "L2CAM" to the Layer 2 path featured in Claim 1. However, L3CAM and L2CAM are merely portions of memory and are not paths as featured in Claim 1.

Furthermore, Claim 1 features a specific function, namely "selecting each route processor of the switched network that" matches three different characteristics, namely that each route processor (a) "is in the Layer 3 path", (b) "appears on the Layer 2 path that is associated with the source device ad the destination device", and (c) "leads to and emanates from the route processor." There is nothing in the cited portions of *Viswanadham* or elsewhere that discloses anything related to such a function for selecting route processors, little less that such route processors are selected based on the three different characteristics enumerated above. All *Viswanadham* discloses is the architecture and operation for a particular design of a multilayer switch.

For at least these reasons, the Applicant respectfully submits that *Viswanadham* does not disclose, teach, suggest, or in any way render obvious "selecting each route processor of the switched network that is in the Layer 3 path and that appears on the Layer 2 path that is associated with the source device and the destination device and that leads to and emanates from the route processor" as featured in Claim 1.

Next, the Office Action states that *Viswanadham* discloses "selecting, for each selected route processor (L3 CAM search), a switch in the network that satisfies a pre-determined set of criteria as a relevant switch engine that multilayer switches the selected route processor (col. 19, lines 41-67; col. 20, lines 1-67; figure 16A)." Yet again, as noted above, the Office Action cites a nearly a column and a half worth of material from

Viswanadham along with a figure without providing reasonable particularity with respect to the basis of the rejections, and as a result, the Applicant has had to engage in guesswork to determine the basis for the rejection.

The cited portion of *Viswanadham* describes Figures 16A and 16B, which illustrate "search operation steps" (Col. 19, line 41) and "CAM lookup steps" (Col. 20, line 38). As discussed above, the CAM is content addressable memory. However, this portion of *Viswanadham* is cited as alleging disclosing the "selecting...a switch" function of Claim 1, specifically the "selecting, for each selected route processor, a switch in the switched network", and there is nothing in the cited portion of *Viswanadham* that discloses any such selection function, little less the selection of a switch for each selected route processor from the previous step in Claim 1.

In addition, the switch selected in Claim 1 is selected because the switch "satisfies a pre-determined set of criteria as a relevant switch engine that multilayer switches the selected route processor." As defined in the Application, a "switch engine" is a "switch that is configured to implement multilayer switching." (Application, page 10, line 22 through page 11, line 1.) Furthermore, as defined in the Application, the "relevant switch engine" is "the switch engine that actually performs the multilayer switching for a particular flow," such as when there are multiple switch engines associated with a route processor. (Application, page 21, lines 17-22.) *Viswanadham* fails to disclose anything about selecting a switch engine, little less a relevant switch engine, as featured in Claim 1. All *Viswanadham* discloses is the architecture and operation for a particular design of a multilayer switch, but *Viswanadham* discloses nothing about the selection of switches for route processors, little less the selection of switches that satisfy the pre-defined criteria as a relevant switch engine.

For at least these reasons, the Applicant respectfully submits that *Viswanadham* does not disclose, teach, suggest, or in any way render obvious "selecting, for each selected route processor, a switch in the switched network that satisfies a pre-determined set of criteria as a relevant switch engine that multilayer switches the selected route processor" as featured in Claim 1.

Finally, the Office Action states that *Viswanadham* discloses "creating and storing information that defines a multilayer switching path and that includes information identifying the source device, destination device, and each selected switch (col. 20, lines 10-13; col. 21,

lines 17-42)." However, the first part of the cited portion of *Viswanadham* merely states "As hardware searches CAM entries and follows linked lists, it stores address of previous entry in register. Entry number is reported with matching entry number in SearchResult registers." (Col. 20, lines 10-13.) Thus, while *Viswanadham* does disclose storing the address of a previous entry in the register in this cited portion, there is nothing in this portion or elsewhere in *Viswanadham* that discloses anything about both "creating and storing information that defines a multilayer switching path," little less that such information "includes information identifying the source device, destination device, and each selected switch" as recited in Claim 1.

The second part of the cited portion of *Viswanadham* describes MAC Address RAM 196 (Col. 21, line 17), that the "L3 results of CAM lookup returned to FE include receive port number and block number originally provided by FE52 and two 16-bit values, L3 Result and L3 Status" (Col. 21, lines 22-24), that "Switch circuit 20 operates on various performance and integrity levels" (Col. 21, lines 27-28), and that "In store forward (SF) mode, receiving packet is not sent to port until reception is complete." (Col. 20, lines 36-37.)

Nothing in this cited portion of *Viswanadham* discloses anything related to "creating and storing information that defines a multilayer switching path" as featured in Claim 1. Furthermore, the last step of Claim 1 also features that the information "includes information identifying the source device, destination device, and each selected switch." Yet the cited portion of *Viswanadham* fails to mention anything about any devices, little less a source device or a destination device, nor is there any mention of the switches that are selected in the third step of Claim 1.

For at least these reasons, the Applicant respectfully submits that *Viswanadham* does not disclose, teach, suggest, or in any way render obvious "creating and storing information that defines a multilayer switching path and that includes information identifying the source device, destination device, and each selected switch" as featured in Claim 1.

(4) CONCLUSION OF DISCUSSION OF CLAIM 1 AND *VISWANADHAM*

Because *Viswanadham* fails to disclose, teach, suggest, or in any way render obvious (a) "determining a Layer 3 path and a Layer 2 path through the switched network from the source device to the destination device," (b) "selecting each route processor of the switched

network that is in the Layer 3 path and that appears on the Layer 2 path that is associated with the source device and the destination device and that leads to and emanates from the route processor,", (c) "selecting, for each selected route processor, a switch in the switched network that satisfies a pre-determined set of criteria as a relevant switch engine that multilayer switches the selected route processor,", or (d) "creating and storing information that defines a multilayer switching path and that includes information identifying the source device, destination device, and each selected switch," the Applicant respectfully submits that, for at least the reasons stated above, Claim 1 is allowable over the art of record and is in condition for allowance.

C. CLAIMS 10, 19, AND 20

Claims 10, 19, and 20 contain features that are the same as those described above with respect to Claim 1, and in particular all feature (a) "determining a Layer 3 path and a Layer 2 path through the switched network from the source device to the destination device," (b) "selecting each route processor of the switched network that is in the Layer 3 path and that appears on the Layer 2 path that is associated with the source device and the destination device and that leads to and emanates from the route processor,", (c) "selecting, for each selected route processor, a switch in the switched network that satisfies a pre-determined set of criteria as a relevant switch engine that multilayer switches the selected route processor,", or (d) "creating and storing information that defines a multilayer switching path and that includes information identifying the source device, destination device, and each selected switch," as in Claim 1. Therefore, based on at least the reasons stated above with respect to Claim 1, the Applicant respectfully submits that Claims 10, 19, and 20 are allowable over the art of record and are in condition for allowance.

D. CLAIMS 2-9, 11-18, 21-28, AND 29-36

Claims 2-9, 11-18, 21-28, and 29-36 are dependent upon Claims 1, 10, 19, and 20, respectively, and thus include each and every feature of the corresponding independent claims. Each of Claims 2-9, 11-18, 21-28, and 29-36 is therefore allowable for the reasons given above for the Claims 1, 10, 19, and 20. In addition, each of Claims 2-9, 11-18, 21-28, and 29-36 introduces one or more additional limitations that independently render it

patentable. However, due to the fundamental differences already identified, to expedite the positive resolution of this case a separate discussion of those limitations is not included at this time. Therefore, it is respectfully submitted that Claims 2-9, 11-18, 21-28, and 29-36 are allowable for the reasons given above with respect to Claims 1, 10, 19, and 20.

However, the Applicant would like to call attention to one issue concerning the rejections of some of the dependent claims. In the rejections of Claims 5-9 and 14-18, the Office Action states that *Viswanadham* fails "to teach establishing the flow between the source device and the destination device by sending packets from any route processor that is upstream from the selected route processor to the destination device when the source device is remote." The Office Action then states that "Stelliga discloses a protocol interaction of one host to remote host (col. 4, lines 20-28, based on OSI model); transferring of data from source to destination on different traffic types (col. 5, lines 56-63; figure 4)." Then the Office Action provides a rationale for combining *Viswanadham* and *Stelliga*.

Although the Applicant is not addressing herein the merits of the rejections of Claims 5-9 and 14-18 for the reasons stated above, the Applicant would like to draw attention to the fact that the Office Action fails to even allege that all the features of any of Claims 5, 6, 7, 8, 9, 14, 15, 16, 17, and 18 are disclosed in *Stelliga*. Instead, the Office Action paraphrases much of Claims 5 and 14 but omits the last phrase (e.g., "during determination of the multilayer switching path"). The Office Action ignores the latter portion of Claims 6 and 15 (e.g., "when the source device is not remote"). The Office Action ignores the latter portion of Claims 7 and 16 (e.g., "wherein the packets that are sent from the network management station traverse the relevant switch engine for the selected route processor"). The Office Action ignores the middle portion of Claims 8 and 17 (e.g., "sending packets from any route processor that is upstream of the selected route processor"). The Office Action ignores both the middle portion of Claims 9 and 18 (e.g., "sending packets from any route processor that is upstream of the selected route processor") and the latter portion of Claims 9 and 18 (e.g., "when the packets that are sent from a network management station do not traverse the relevant switch engine for the selected route processor"). Thus, it does not appear to the Applicant that the Office Action has identified anything in either *Viswanadham* or in *Stelliga* that allegedly discloses the omitted features of Claims 5, 6, 7, 8, 9, 14, 15, 16, 17, and 18.

CONCLUSION

The Applicant believes that all issues raised in the Office Action have been addressed and that allowance of the pending claims is appropriate. After entry of the amendments, further examination on the merits is respectfully requested.

The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

For the reasons set forth above, it is respectfully submitted that all of the pending claims are now in condition for allowance. Therefore, the issuance of a formal Notice of Allowance is believed next in order, and that action is most earnestly solicited.

To the extent necessary to make this reply timely filed, the Applicant petitions for an extension of time under 37 C.F.R. § 1.136.

If any applicable fee is missing or insufficient, throughout the pendency of this application, the Commissioner is hereby authorized to any applicable fees and to credit any overpayments to our Deposit Account No. 50-1302.

Respectfully submitted,
HICKMAN PALERMO TRUONG & BECKER LLP

Dated: June 25, 2004

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Attachment - Copy of Response to Notice to File Missing Parts with Executed Declaration

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